



VIETNAM NATIONAL UNIVERSITY OF HO CHI MINH CITY
UNIVERSITY OF NATURAL SCIENCES
FACULTY OF INFORMATION TECHNOLOGY

COURSE SYLLABUS

Course Code:	TH101
Title:	Computer Architecture
Credits:	2
Workload:	Lecture hours: 2 periods * 15 weeks = 30 periods No laboratory work Preparative hours:
Prerequisites:	TH010 or TH011 - Introduction to Computer Science A1

Course Objectives:

This course introduces the fundamental concepts of computer architecture. It is a one-semester essential course for computer science students. Topics include: fundamental digital components, major categories of computers, various measures of computer performance, building blocks of computers (instruction set, hardware system, CPU, input-output system, and memory system), architecture of the IBM-PC family, pipelining and reduced-instruction-set computers, and parallel processors.

Main Text: N/A

References:

- *Computer Architecture*, Robert J. Baron, Lee Higbie.-USA: Addison-Wesley, 1992.
- *Computer Organization and Assembly Language Programming for IBM PCs and Compatibles.-2nd ed*, Michael Thorne.-Singapore: Benjamin/Cummings, 1991.
- *Turbo Assembler Bible*, Gary Syck.-USA: SAMS, 1991.
- *Computer Organizations and Design (The Hardware/Software Interface)*, David A. Patterson and John L. Hennessy, 3rd edition, Morgan Kaufmann, 2005.

Course Outline:

Chapter 1 Basic digital circuits

- 1.1 Circuit components
 - 1.1.1 Bus
 - 1.1.2 Gate
- 1.2 Combinational Logic
 - 1.2.1 Encoder and Decoder
 - 1.2.2 Multiplexors and Demultiplexors
 - 1.2.3 Shift Register
 - 1.2.4 Adder

1.2.5 Arithmetic and Logical Unit (ALU)

1.3 Sequential Logic

1.3.1 Flip-Flop Circuits

1.3.2 Clock Circuitry

1.3.3 Registers and Counter Circuits

1.4 Devices include both Combinational and Sequential Logic

1.4.1 Register Set

1.4.2 Hard Stack

1.4.3 Multiplier Circuit

Chapter 2 Computer Architecture

2.1 Overview

2.2 History

2.3 Classify Computer Architectures

2.3.1 Von Neumann machines

2.3.2 Non-Von Neumann machines

2.4 Evaluation of a Computer Architecture

2.4.1 Popularity

2.4.2 Applicability

2.4.3 Efficiency

2.4.4 Ease of Use

2.4.5 Malleability

2.4.6 Expandability

2.5 Factors influencing the success of a computer architecture

2.5.1 Architecture Merit

2.5.2 System performance

2.5.3 System cost

Chapter 3 Instruction Set Architecture

3.1 Data Representation

3.1.1 Units of Information

3.1.2 Integers and Fractions

3.1.3 Floating Point Numbers

3.1.4 Data Structures

3.2 Data Precision and Data Types

3.2.1 Precision of Basic Data Types

3.2.2 Provision of Variable-Precision Data

3.3 Register Sets

3.4 Types of Instructions

3.4.1 Operate Instructions

3.4.2 Memory-Access Instructions

3.4.3 Control Instructions

3.4.4 Miscellaneous and Privileged Instructions.

3.4.5 Vector Instructions

3.5 Addressing Techniques

- 3.5.1 Register Addressing
- 3.5.2 Boundary Alignment
- 3.5.3 Memory Addressing
- 3.5.4 Addressing Design Issues
- 3.6 Instruction-Set Design
 - 3.6.1 Completeness
 - 3.6.2 Orthogonality
 - 3.6.3 Compatibility
 - 3.6.4 Instruction Formats

Chapter 4 Buses, the CPU, and the I/O system

- 4.1 Buses
 - 4.1.1 Bus Types
 - 4.1.2 Bus Transfers and Control Signals
- 4.2 Central Processing Unit
 - 4.2.1 ALUs
 - 4.2.2 Control Units
 - 4.2.3 Exception-Processing Hardware and Instructions
- 4.3 I/O System
 - 4.3.1 CPU-Controlled I/O
 - 4.3.2 Multiprogramming Operating Systems
 - 4.3.3 Multi-Ported Storage
 - 4.3.4 DMA I/O
 - 4.3.5 Memory-Mapped I/O
 - 4.3.6 Physical I/O Devices

Chapter 5 Memory-System Architecture

- 5.1 Memory-System Technology
 - 5.1.1 Memory Organizations
 - 5.1.2 Types of Memory
- 5.2 Main Memory System
 - 5.2.1 Program Relocation and Protection
 - 5.2.2 Cache Memory
 - 5.2.3 Virtual Memory
 - 5.2.4 Memory Banking and Expanded Memory
- 5.3 Memory Design Issues
 - 5.3.1 Memory Speed versus CPU Speed
 - 5.3.2 Memory-Address Space
 - 5.3.3 Speed-Cost Tradeoffs

Chapter 6 A computer-family architecture : the IBM PC

- 6.1 IBM PC Family and Its Descendants
 - 6.1.1 IBM PC and PC AT
 - 6.1.2 IBM PS/2

- 6.1.3 PC Clones
- 6.2 Basic Microcomputer Configuration
- 6.3 Components of the IBM PC
 - 6.3.1 8088 CPU
 - 6.3.2 Control Interface
 - 6.3.3 PC Bus And Interrupt System

 - 6.3.4 I/O System
 - 6.3.5 Programmable Interval Timer
 - 6.3.6 Floating-Point Coprocessor
- 6.4 Software System
 - 6.4.1 I/O Port-Address Assignments
 - 6.4.2 ROM BIOS
 - 6.4.3 Memory-Address Assignments
- 6.5 Architectural Merit of the PC Architecture

Chapter 7 Pipelining and RISCs

- 7.1 Pipelining
 - 7.1.1 Arithmetic-Unit Pipelining
 - 7.1.2 Instruction-Unit Pipelining
 - 7.1.3 Scheduling Functional Units
- 7.2 Pipelined Vector Processors
- 7.3 Reduced-Instruction-Set Computers
 - 7.3.1 Historical Perspective
 - 7.3.2 RISC-CISC Controversy
 - 7.3.3 RISC Implementation Techniques

Chapter 8 Parallel Processors

- 8.1 Interconnection Networks
 - 8.1.1 Taxonomy
 - 8.1.2 Interconnection Topologies
 - 8.1.3 Application of Interconnection Networks for Parallel Processors
- 8.2 SIMD Machines
 - 8.2.1 Types of SIMD Architectures
 - 8.2.2 SIMD Operations
- 8.3 MIMD Machines
 - 8.3.1 Running Processes on a MIMD Processor
 - 8.3.2 Requirements for Multi-Processor System
 - 8.3.3 Cache Coherence
 - 8.3.4 Loosely Coupled Multiprocessors
 - 8.3.5 Fault-Tolerant Computers
- 8.4 Other Architectures
 - 8.4.1 Dataflow
 - 8.4.2 Neural Networks

Grading

Final exam :

Assignments: